Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A System comprising:

a first processor bus;

a first processor on a first clock coupled to the first processor bus;

a first direct memory access unit with a first external direct memory access channel, the first direct memory access unit being coupled to the first processor bus;

a first programmable unit comprising a first processor interface, the first programmable unit coupled via the first external direct memory access channel to the first direct memory access unit, said first programmable unit being programmable by the first processor via the first processor interface;

a first shareable unit coupled to the first processor bus;

a second processor bus;

a second processor on a second clock coupled to the second processor bus;

a second direct memory access unit with a second external direct memory access channel, the second direct memory access unit being coupled to the second processor bus;

a second programmable unit comprising a second processor interface, the second programmable unit coupled via the second external direct memory access channel to the second direct memory access unit, said second programmable unit being programmable by the second processor via the second processor interface; and

a second shareable unit being connected to the second processor bus,

wherein the first programmable unit and the second programmable unit each comprises:

a direct access unit core;

a first external direct memory access channel interface on the first clock; and

a second external direct memory access channel interface on the second clock,

wherein a first bi-directional communication channel is established between the first shareable unit and the second processor via the first programmable unit, and a second bi-directional communication channel is established between the second shareable unit and the first processor via the second programmable unit.

2. (Previously Presented) The system of claim 1, wherein the first bi-directional communication channel and/or the second bi-directional communication channel are half-duplex channels or full-duplex channels.

3. (Previously Presented) The system of claim 1, wherein the first processor and the second processor are similar from an architectural point of view.

4. (Previously Presented) The system of claim 1, wherein the first processor and the second processor are implementations of the same type of processor design.

5. (Previously Presented) The system of claim 1, wherein the first processor and the second processor are implementations of different types of processor design.

6. (Previously Presented) The system of claim 1, wherein the first and second shareable units each comprise one of the following: a memory, a peripheral, an interface, an input device, an output device.

7. (Previously Presented) The system of claim 1, wherein one of the first and second processors comprises a central processing unit, a microprocessor, a digital signal processor, a system controller, a co-processor, or an auxiliary processor.

8. (Canceled)

9. (Previously Presented) The system of claim 1, wherein each processor interface has a programming link either for connecting to a corresponding processor bus or for connecting to a corresponding processor.

10. (Previously Presented) The system of claim 1, wherein the first and second bi-directional communication channels are configured to transfer data and/or control information to and from the first and second shareable units.

11. (Canceled)

12. (Canceled)

13. (Currently Amended) A system comprising:

a first processor and a first shareable unit coupled to a first bus, the first processor and first shareable unit operating on a first processor clock;

a second processor and a second shareable unit coupled to a second bus, the second processor and second shareable unit operating on a second processor clock;

a first bi-directional channel to couple the second processor to the first shareable unit via the first and second busses, the first bi-directional channel configured to decouple the clock domain of the second processor from the clock domain of the first shareable unit, the first bi-directional channel also coupled through a first programming interface to the second ~~processor;~~ processor, wherein the first bi-directional channel comprises:

a first internal channel of a first DMA unit coupled to the first bus, the first DMA unit configured with a first external channel to operate on the first processor clock; and

a first internal channel of a second DMA unit coupled to the second bus, the second DMA unit configured with a first external channel to operate on the second processor clock; and

a second bi-directional channel to couple the first processor to the second shareable unit via the first and second busses, the second bi-directional channel configured to decouple the clock domain of the first processor from the clock domain of the second shareable unit, the second bi-directional channel also coupled through a second programming interface to the first processor, the second bi-directional channel being simultaneously operable with the first bi-directional channel between the first and second ~~bus.~~ bus, wherein the second bi-directional channel comprises:

a second external channel of the first DMA unit to operate on the first processor clock; and

a second external channel of the second DMA unit to operate on the second processor clock.

14. (Currently Amended) The system of claim 13, wherein the first bi-directional channel comprises:

~~a first internal channel of a first DMA unit coupled to the first bus, the first DMA unit configured with a first external channel to operate on the first processor clock;~~

~~a first internal channel of a second DMA unit coupled to the second bus, the second DMA unit configured with a first external channel to operate on the second processor clock; and~~

a first programmable unit coupled between the first external channel of the first DMA unit and the first external channel of the second DMA unit, the first programmable unit comprising the first programming interface to the second processor, the first programmable unit also configured to decouple the second processor clock from the first processor clock.

15. (Currently Amended) The system of claim 14, wherein the second bi-directional channel comprises:

~~a second external channel of the first DMA unit to operate on the first processor clock;~~

~~a second external channel of the second DMA unit to operate on the second processor clock; and~~

a second programmable unit coupled between the second external channel of the first DMA unit and the second external channel of the second DMA unit, the second programmable unit comprising the second programming interface to the first processor, the second programmable unit also configured to decouple the second processor clock from the first processor clock.

16. (Currently Amended) The system of claim 13, wherein the first bi-directional channel comprises:

~~a first internal channel of a first DMA unit coupled to the first bus, the first DMA unit configured with a first external channel to operate on the first processor clock;~~

~~a first internal channel of a second DMA unit coupled to the second bus, the second DMA unit configured with a first external channel to operate on the second processor clock;~~

a first external channel of a common programmable unit, the first external channel operating on the second processor clock, and the first external channel also coupled to the first external channel of the second DMA unit;

a second external channel of the common programmable unit, the second external channel to operate on the first processor clock, and the second external channel also coupled to the first external channel of the first DMA unit; and

a first programmable core of the common programmable unit, the first programmable core to operate on the second processor clock, the first programmable core coupled between the first and second external channels of the common programmable unit and the first programmable core comprising the first programming interface to the second processor.

17. (Currently Amended) The system of claim 16, wherein the second bi-directional channel comprises

~~a second external channel of the first DMA unit to operate on the first processor clock;~~

~~a second external channel on the second DMA unit to operate on the second processor clock;~~

a third external channel of the common programmable unit, the third external channel to operate on the second processor clock, and the third external channel also coupled to the second external channel of the second DMA unit;

a fourth external channel of the common programmable unit, the fourth external channel to operate on the first processor clock, and the fourth external channel also coupled to the second external channel of the first DMA unit; and

a second programmable core of the common programmable unit, the second programmable core to operate on the first processor clock, the second programmable core coupled between the third and fourth external channels of the common programmable unit and the second programmable core comprising the second programming interface to the first processor.

18. (Previously Presented) The system of claim 13, wherein the first bi-directional channel further comprises a first master configured to initiate data transfers with active devices on the first or second busses.

19. (Previously Presented) The system of claim 13, wherein the second bi-directional channel further comprises a second master configured to initiate data transfers with active devices on the first or second busses.

20.-23. (Canceled)